

## Abstract

A pipelined sample-and-hold circuit is provided. The circuit is pipelined such that processing of a held signal can continue into the next sample phase. Also, the pipelined sample-and-hold circuit includes a hold switch. The hold switch includes a boosted switch and dummy circuits. The boosted switch circuit is responsive to a boosted signal. The dummy circuits are arranged for charge injection cancellation responsive to another boosted signal that is a substantially inverse of the boosted signal.

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